

MASTER_3D

MANufacturing Solutions Targeting competitive European pROduction in 3D

General description

The project MASTER_3D aims at reaching excellence in 3D IC production by developing and implementing methods to enable cost competitive manufacturing. The activities focus on 3D ICs with Through Silicon Vias (TSV) and Wafer Level Packaging (WLP).

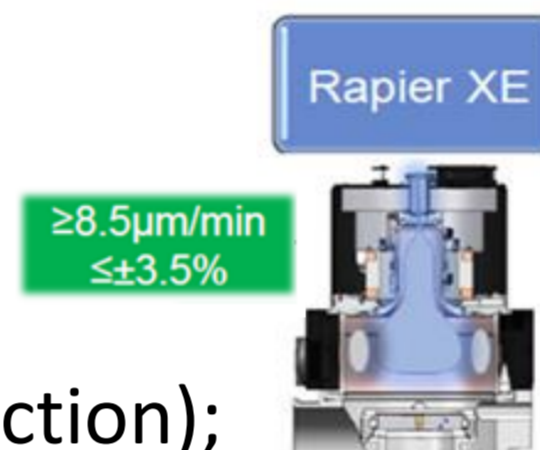
Goals / Objectives

- Process tools investigation, assessment and improvement to support high yield production
- Improved unit processes including identification of major cost driver for reliable production
- Failure analysis methods and tools in mass production environment
- Characterization and metrology methods and tools
- Test infrastructure and strategy
- Yield modelling and improvement
- Verification based on test vehicles

Societal impact / Results

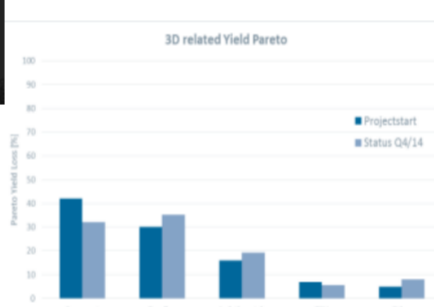
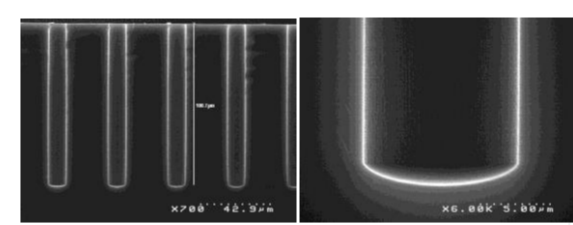
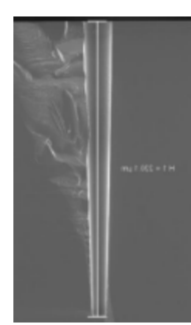
World leading equipment achievements for 3D

- SPTS: Via reveal etch rate improvement with SPTS Rapier XE tool (CoO reduction); MoCVD barrier deposition step coverage enhancement for CoO reduction
- EVG: Room temperature debonding of ultra thin wafers (chuck with IZM ASSID)



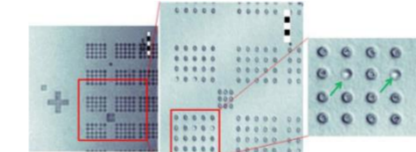
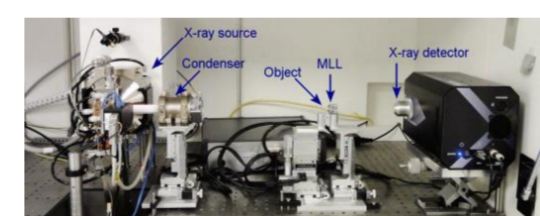
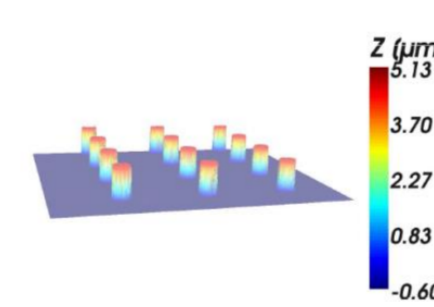
World leading processes for 3D achievements (highlights)

- IFAG: Etching that allows to reduce scallops
- ALES & CEA-LETI: Cost-effective and competitive ECD Cu-fill chemistry
- STMicro: Defect free TSV middle etching process ready and Cu-pillars (e.g. pillar height measurements together with CEA-LETI)
- ams: Yield learning and built up of an effective failure analysis environment; improved yield in sensor production will be demonstrated at the project end.
- Rockwood: Qualification of a new down sizing process to sustain small diameter wafers (e.g. SOI); improvements measured on production lots on CMOS wafer preparation before bonding
- Qualtera: Data structure for Fab-to-Final Test 3D part traceability and data alignment, as well as platform for predictive 3D parametric and yield modeling ready
- NXP and FhG IZM ASSID: Collaboration on a 3D-security system based on near field communication with focus on new advanced and cost efficient TSV processing, SPC data evaluation etc.
- FhG IZM ASSID & EVG: Development of a new wafer de-bond chuck for temporary zone bond
- FhG and Sentronics: Collaboration on remaining Si thickness (RST) measurements



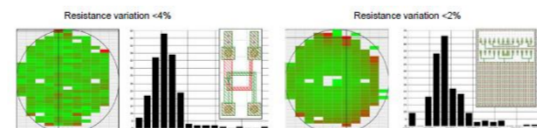
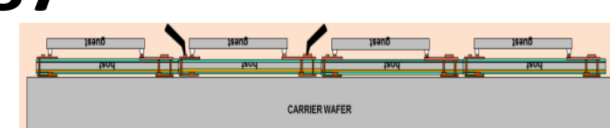
World leading characterization/metrology tools for 3D achievements

- Fogale: Development of T-MAP DUAL 3D fully completed
- Sentronics: SemDex is the most flexible fully-automated semiconductor metrology system for 3D IC
- AXO & FhG IKTS: Portable X-ray microscopy set-up ready
- PVA Tepla, supported by FhG IWMH and IMS: World leading automated high throughput SAM



World leading 3D test strategy

- FhG IZM ASSID and NXP, together with CEA-LETI and LIRMM, who worked on design for testability at system level and wafer level














The Master_3D team: A partnership to drive European 3D System Integration

Master_3D: A wealth of Know How

- New process capabilities for 3D
- New process equipments for 3D
- New characterization equipments & metrology for 3D
- New testing capabilities for 3D
- New test vehicles to demonstrate technologies

Partners

- Air Liquide Electronics Systems 
- ams AG 
- AXO DRESDEN 
- Commissariat à l'Énergie Atomique 
- EV Group 
- Fraunhofer Gesellschaft (IZM ASSID, IWMH, IKTS) 
- Fogale Nanotech 
- Infineon 
- IMS Bordeaux 
- Sentronics Metrology 
- Laboratoire d'Informatique, Robotique et Microélectronique Montpellier 
- NXP Semiconductors 
- PVA TePla Analytical Systems 
- Qualtera 
- Rockwood Wafer Reclaim SAS 
- SPTS Technologies 
- STMicroelectronics 

Countries involved

- Austria
- France
- Germany

Examples for exploitation

SPTS, EVG: unit process equipments ready for entering the market
 Fogale, Sentronics, PVA Tepla: characterization equipment ready for entering market
 For ST, NXP, ams, and IFAG environment set up for 3D processing
 ST: New processes applicable for Si photonics, advanced logic to create new opportunities.
 ams: ready for sensor volume production
 IFAG: A first toolbox for TSV fabrication investigated and ready for dedicated applications

Additional information

Project start date: December 1st, 2012
 Duration: 3 years (German partners until June 2016)
 Dissemination: > 40 publications; 2 patents
 1 international award: "3D incities award"