FOWLP Goes Mainstream. PVD Solutions for the Fastest Growing Packaging Format

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Contents

- The rise of FOWLP
  - Why it’s needed
  - Examples
  - Market growth
- PVD processing of FOWLP
  - Challenges – contamination, particles, Cu exposed area
  - Solutions
The Interposer Gap: Line & Space

- PCB Substrate Manufacturers
- OSAT / Wafer foundries
- Silicon
- Opportunity
- FanOut
- GAP!
- Organic Substrate
- Glass
- Who manufactures interposers? Ground rules?
- Lower cost than Si/Glass Interposer?
- eWLB: <10um L/S
- TSMC INFO: <5um L/S
- RDL first FO: <2um L/S
- Wafer Design Rule

100µm 25µm 10µm ~8-> 5µm 1µm 100nm 10nm

Courtesy Phil Garrou, Yole
FOWLP Examples In Production

- Original Infineon eWLB, Single Die
  - Wireless Baseband SoC (GPS, FM Radio, BT)

- Multi-Chip Modules, Integrated Passives

- 10 µm L/S
- Up to 3 Metal Levels (2 x RDL, 1 x UBM)

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Increasing I/O Density

Amkor SWIFT
[Silicon Wafer Integrated Fan-out Technology]

Amkor SLIM
[Silicon-Less Integrated Module]

TSMC InFO
[Integrated Fan-Out]

SPIL SLIT
[Silicon-Less Interconnect Technology]

Fan-Out Programs in OSATs & Foundries Increasing

Courtesy of Amkor
Jun 15: Yole’s View of FOWLP Market
Sep 15: The TSMC Effect

With TSMC, 10x bigger market by 2020
Other Analysis is Available…

- Started with baseband processors
- Multiple applications appearing now
  - RF, NFC, GPS, PMIC, auto radar
  - APU
  - Memory

Chip-First
- eWLB, aWLP, WLFO (Infineon, ICET STATS ChipPAC, ASE, NANIUM)
- RCP (Freescale/NXP, Napes)
- M-Series (DECA)
- InFO (TSMC)
- WLFO (Amkor)
- ADL/SinoChip
- FOWLP (SPIL)
- NTI (SPIL)
- WFP (Samsung)

Chip-Last
- FOCLP (ASE)
- SWIFT (Amkor)
- SLIM (Amkor)
- RDL-First FOWLP (IME)
- HDL (QPL)
- FC-MISBGA (SPIL)
- EMIB/Si-Bridge (Intel)

Source: TechSearch International, Inc.

130% CAGR in units, ‘15 to ’19
PVD Processing of FO Wafers
PTOR for original eWLB R&D

HVM since 2009
  - >> 1M wafers processed
  - 200 mm, 300 mm & 330 mm

Multiple customers:
  - R&D, Production
RDL Processing on FOWLP

Multiple challenges for PVD:

- Contamination: mold contains moisture, solvents
  - Must be removed before metal dep otherwise high Rc
  - Problem: mold wafer max temperature is low, <150°C

- Particles
  - Organic dielectrics commonly used in packaging; PBO, PI
  - Problem: carbon by-products can flake from chamber furniture after preclean

- Large Cu exposed area on top RDL
  - Problem: stops RF penetration in ICP etch chambers

- Mold wafer is not flat
  - We modify furniture clearances, robot profiles, temperature rise & fall rates
Water and CO dominate
At 120C, takes @30mins for gases to approach pre-load values
How manage and still be productive?

Mold Contains Contaminants

- Water and CO dominate
- At 120C, takes @30mins for gases to approach pre-load values
- How manage and still be productive?
Degas Under High Vacuum Is Key

- To achieve lowest Rc, highest yield, degas under vacuum
- Degassing ex-situ and move to PVD system less effective
  - Mold quickly re-absorbs
  - Changes in transfer time will cause variable results

![Graph showing outgas rates for different degas conditions](image)

In-situ degas design ensures lowest outgas rates
T’put Advantage Using MWD

- Mold contains moisture, and has low temperature tolerance
  - Must degas for long time = throughput bottleneck
- Solution = Multi-Wafer Degas (MWD)
  - Batch concept, removes degas bottleneck
- Cryopumped for water efficiency
- Attached to the high vacuum side
- Complex scheduling software
  - Manages batch/single wafer interaction
Benefit of MWD – High Throughput

Tests performed on FO-WLP Epoxy Mold Compound Test Vehicle
TMAX = 120°C

Individual wafers get long degas
Degas in parallel means t’put stays high
Dealing With I/O Density Increase

- FOWLP I/O density increasing, reduced L/S patterning
  - Increasing area of exposed metal
- In an ICP pre-clean, metal deposited onto the ceramic will block RF
  - Plasma eventually turns off

How do you keep the lights on?

High exposed Cu on Standard ICP
Cu builds up on ceramic wall
Etch rate falls away
**SE-LTX Solution**

- Modified design prevents continuous band of metal forming on the wall
- Stability maintained over 5000 wafers

![Graph showing Etch Rate (Å/min) vs Wafer number](chart1)

- PLUS allows metal pasting for PI/PBO particle control...

![Graph showing Added Particles vs Wafer number](chart2)
Keeping $R_c$ Low

- Polymer dielectric passivation
  - PI, PBO, BCB, WPR
- Ion bombardment during pre-clean
  - Removes native oxide from bondpad
  - But also...breaks down polymer crust
  - C by-products and moisture released
  - Pad metal becomes contaminated
  - $R_c$ increases

- Shrinking CD’s increase the challenge
CO Peaks vs Competitor Diode Etch

ICP vs CCP (Diode Etch)

Significantly Lower CO Released Using ‘Soft Etch’ Approach
Stable Rc

- If not controlled, CO pp will rise during batch
  - Time to pump away >> process time per wafer
  - Result: Rc rises through batch
- In SE-LTX, Rc stays in control – CO pp not rising
Summary

- **FOWLP is the fastest growing packaging format**
  - High density and cost benefits
  - 5um L/S production ready, 2um capability proven

- **Multiple challenges for PVD vendor**
  - Contamination can compromise Rc
  - Particles from re-deposited organics
  - Large Cu exposed area impacts conventional ICP designs
  - Warpage

- **Simply adapting existing systems not sufficient**

- **Solutions required new thinking, validated in production**
  - Low Rc at high throughput
  - High uptime from long life SE-LTX
  - Low wafer breakage