Dielectric Stack Engineering for Via-Reveal Passivation

Kath Crook, Mark Carruthers, Daniel Archard, Steve Burgess, Keith Buchanan
SPTS Technologies.
Ringland Way, Newport NP18 2TA, United Kingdom.
keith.buchanan@spts.com

Abstract
This paper reports on the development of low temperature (<190°C) plasma-enhanced chemical vapour deposition (PECVD) processes used to deposit dielectric films for use as passivation layers over wafer back side revealed vias in thinned (<60µm), 300mm silicon wafers.

Introduction
Wafer back side processing is a critical link in the 3D-IC wafer stacking process flow. Through-silicon vias [TSV], typically formed using ‘via-middle’ processing with 300-400°C thermal budget, are exposed from the back sides of 300mm wafers by grind and plasma etch steps. Dielectric layers deposited using PECVD serve to passivate and mechanically support the exposed TSV prior to bump/RDL formation and then chip-to-wafer or wafer-to-wafer bonding.

Prior to via-reveal processing, device wafers are bonded to silicon or glass carriers and thinned to around 50µm. The temporary bonding material imposes a temperature constraint and wafer temperatures must not exceed ~190°C during all subsequent via-reveal process steps. The temperature constraint is especially challenging for the PECVD passivation processes where films with stable electrical and mechanical properties are required.

The PECVD passivation process is also critical for the control of wafer bow. Full thickness (~770µm), incoming wafers from CMOS front-end wafer fabs typically have wafer bow of ~150µm or less. When the incoming wafer is thinned to ~50µm to allow chip stacking, bow will increase to several centimetres. Such large bows make wafer handling impossible and can also cause cracking after debond. The back side PECVD dielectric passivation films can be tailored to compensate for the incoming wafer stress and so produce wafers with manageable flatness after debond. To achieve this, low temperature PECVD SiO and SiN films having both compressive and tensile stresses must be available. In particular, CMOS devices incorporating multiple layers of low k dielectric will typically have a front side tensile stress and so via-reveal passivation stacks with net tensile stress are required to compensate. Engineering of low temperature (<190°C) PECVD SiO with tensile stress, low leakage current and adequate stability and cracking threshold is extremely challenging as these films are typically susceptible to water re-absorption on exposure to atmosphere [1,2].

In this paper, we report on dielectric stack engineering for via-reveal passivation. Optimized SiN-SiO stacks deposited at <190°C give excellent electrical properties with leakage current densities <1E-9 A.cm-2 and breakdown voltages >10 MV.cm-1. Crucially, electrical properties and stack stress are shown to be stable with no drift over time when exposed to atmosphere. Stack stress engineering is discussed; compressively stressed SiN barrier films are combined with tensile SiO and SiN over layers to produce stacks optimized for reliability and having a net tensile stress. Modelled stack stress data is shown to be in good agreement with measured data. Stack optimization is discussed with a view to providing stress compensation for wafers with either tensile or compressive incoming stress.

Experimental
Dielectric films were deposited on to 300mm Si wafers using an SPTS Delta fxp, single-wafer cluster system designed for high volume manufacturing and configured with multi-wafer degas (MWD) and PECVD chambers. The MWD chamber uses infra-red lamps to heat multiple 300mm wafers in a cassette within the chamber. This batch heating approach allows for degas times of up to 30 minutes with minimal effect on PECVD system throughput. For bonded (silicon-on-silicon or silicon-on-glass) substrates used during via-reveal processing, long degas times are required to ensure that the

Figure 1. Typical via-reveal process flow.
bonding adhesive is sufficiently outgassed prior to dielectric stack deposition. Failure to do this will result in outgassing occurring during the deposition step with consequent disruption of plasma stability and degradation of film properties. Figure 2 shows outgassing characteristics typical of a bonded, silicon-on-glass substrate. In this example, outgassing was measured in a PECVD chamber with wafers sitting on 180°C platen with base pressure of approximately 20mTorr. Peak wafer temperature was <150°C. The outgassing rate peaks after ~100 seconds but it takes 6-8 minutes for the pressure to recover to a value close to that of chamber base pressure.

![Figure 2. Typical out-gassing characteristics of bonded wafers](image)

Figure 3 shows a PECVD cluster system configured with a single Multi-Wafer Degas chamber serving five PECVD chambers.

![Figure 3. PECVD cluster system with Multi-Wafer Degas chamber and 5 PECVD chambers](image)

SiN and SiO films were deposited in a capacitively-coupled, parallel plate PECVD reactor. Reactant gases enter the chamber through a showerhead whose design is optimized to give <3% within-wafer thickness uniformity for both silicon oxide and silicon nitride on 300mm wafers.

The wafers sit on a resistively heated platen during deposition with platen temperature adjusted to maintain a wafer temperature of <190°C, this being required to prevent premature debond of the silicon wafer from its temporary carrier. Peak wafer temperature is verified using thermally sensitive adhesive dots applied to the front sides of the substrates prior to deposition. This approach gives a truer indication of peak wafer temperature as it includes film deposition, unlike thermocouple-based temperature measurement techniques. The thermally sensitive dots have a sensitivity of ±3°C within the temperature range 180°C to 200°C. The wafer platen also features active air cooling to prevent energy from the plasma from overheating the wafer and platen assembly during deposition, and also during plasma cleaning of the PECVD chamber. Platen heating and cooling are both controlled by the system software and ensure that platen temperature remains within ±1°C of set point.

SiN-SiO stacks were deposited sequentially in the same PECVD chamber. Such an approach is preferred for best system productivity.

Silicon nitride films are deposited using a silane-based, ammonia-free process chemistry and 13.56 MHz excitation frequency. Film stress is tunable from -400 MPa to +200 MPa where a negative stress denotes a compressively stressed film. Use of 13.56 MHz (compared to low or mixed frequency processes using 375-380 kHz excitation) avoids excessive ion bombardment of the film and so enables high deposition rates without causing overheating of the substrate. This is especially important for bonded substrates where thermal conduction to the wafer platen is significantly reduced compared to a non-bonded silicon wafer.

Silicon oxide films are deposited using a TEOS-based chemistry and dual frequency excitation (13.56 MHz and 375 kHz applied simultaneously to the showerhead). TEOS is preferred to silane as the primary precursor because of its superior step coverage. SiO stress is tunable from -200 MPa to +200 MPa. To ensure compatibility with silicon-on-glass substrates where the carrier is electrically insulating, the lower frequency (375 kHz) power is limited to ≤25% of total RF power. For this work, the SiO deposition process is optimized to prevent absorption of moisture from atmospheric exposure. SiO films deposited using TEOS at low temperature can be hygroscopic and the water absorption causes instability with leakage current and stress drifting upwards over time.

Average thickness and uniformity of individual SiO and SiN films, and also film stacks was measured using a 49-point ellipsometry measurement with 3mm edge exclusion. Stress was calculated using a laser-based bow measurement system. The electrical leakage current density and breakdown voltage of the dielectric films were measured at room temperature using a metal-insulator-semiconductor (MIS) structure with low resistivity silicon as the lower electrode and evaporated aluminium dots with ~1.5mm diameter as the upper electrodes. Leakage current was measured at 2MV.cm⁻¹ electric field strength and breakdown voltage was measured on 150nm SiO and SiN films with voltage swept from 0V to 200V in 5V increments.

Film hardness and elastic modulus were measured by nano-indentation and adhesion was assessed using by diamond-scribing a 10x10 grid into the deposited film and then using adhesive tape pull. Finally, film thickness cracking threshold was determined by using a diamond tip to score the film at the centre and edge of a 300mm wafer. An optical microscope is then used to check for crack propagation over a period of ~24 hours. Observation of spontaneous crack propagation was seen as confirmation that the cracking threshold had been exceeded.
Wafer bow modeling

The modified Stoney equation was used to calculate wafer radius of curvature of the bowed wafer from measured stress:

\[
\sigma_f = \frac{E_s t_s^2}{6 R t_f}
\]

\(\sigma_f\) = film stress

\(E_s\) = biaxial Young’s modulus for the substrate material where \(E_s = E_s^0 / (1 - \nu_s^0)\) and \(E_s^0\) and \(\nu_s^0\) are elastic modulus and Poisson’s ratio respectively.

\(T_s\) = substrate thickness

\(T_f\) = film thickness

\(R\) = radius of curvature

Calculated values or radius of curvature are then used to calculate bow of 300mm wafers using simple trigonometry. Bow is estimated using the equation:

\[
b = \frac{r^2}{2R}
\]

This assumes that the bowed wafer can be modeled as triangular as shown in Figure 4.

![Figure 4](image)

**Figure 4.** Schematic defining wafer bow (b) and radius of curvature (R).

The bow model accuracy was tested by comparing predicted and measured bows for a number of SiN-SiO film stacks typical of those used for via-reveal passivation. Full thickness silicon wafers were used and substrate thickness was measured for each wafer, together with film thickness and stress.

<table>
<thead>
<tr>
<th>SiN Thickness (µm)</th>
<th>SiN Stress (MPa)</th>
<th>TEOS Thickness (µm)</th>
<th>TEOS Stress (MPa)</th>
<th>Stack Thickness (µm)</th>
<th>Waf er Thickness (µm)</th>
<th>Stack Thickness (µm)</th>
<th>Measured Bow (µm)</th>
<th>Modeled Bow (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>200</td>
<td>2.2</td>
<td>66</td>
<td>3</td>
<td>720</td>
<td>3.06</td>
<td>70.0</td>
<td>73.0</td>
</tr>
<tr>
<td>0.3</td>
<td>200</td>
<td>2.2</td>
<td>150</td>
<td>2.5</td>
<td>725</td>
<td>2.55</td>
<td>92.2</td>
<td>92.0</td>
</tr>
</tbody>
</table>

**Table 1.** Predicted vs measured film stress

The results are shown in Table 1 and there is less than 5% differenced between measured and modeled bow.

Dielectric stack engineering

Requirements of the films and processes used for via-reveal passivation can be summarized as below:

1. Peak wafer temperature during deposition compatible with the bonding adhesive used – typically <190°C.
2. Processes must be compatible with silicon, silicon-on-silicon and silicon-on-glass substrates.
3. Complete out-gassing of the bonding adhesive prior to film deposition.
4. Stability – no changes to leakage current or stress after deposition.
5. Highly uniform films to minimize total thickness variation (TTV) of the substrate.
6. Good sidewall coverage of the revealed TSV with no corner voiding
7. Good electrical isolation – leakage current densities <1E-9 A.cm².
8. Breakdown electric field >8MV.cm⁻¹ for reliability.
9. Good diffusion barrier performance – prevention of impurity diffusion to the active silicon
10. Good interfacial adhesion of the passivation stack to silicon and also within the stack itself, where large stress gradients may exist.
11. Tunable film stress to allow for bow compensation on thinned silicon.
12. Thickness cracking threshold – compatible with required overall stack thickness, typically 2.5-3.0µm.
13. Hardness and elastic modulus compatible with subsequent Chemical Mechanical Planarization (CMP) process.

A silicon nitride film with compressive stress is generally acknowledged to give best diffusion barrier properties, such films being widely used in CMOS multi-level metal interconnect schemes [3]. For the via-reveal passivation stack, a PECVD SiN process with peak wafer temperature <190°C and film stress of -100 MPa was developed for this purpose.

For wafers with an incoming front side compressive stress, a compressively stressed TEOS over-layer can be used to provide stress compensation and good sidewall coverage of the revealed TSV.

When the incoming front side stress is tensile, then given the constraint of a compressively stressed SiN barrier layer, it is necessary to deposit thicker over-layers with tensile stress to produce a passivation stack with net tensile stress. SiN and SiO films can both be deposited with a tensile stress and the two films have both advantages and disadvantages for via-reveal process integration.

TEOS-based silicon oxide films deposited in the tensile stress regime have superior sidewall coverage and deposition rate compared to silicon nitride, but maximum thickness is limited by the cracking threshold.
Figure 5 plots the maximum thickness before spontaneous cracking occurs (cracking threshold) vs film stress for low temperature TEOS SiO films. Maximum film thickness is less than 2µm for film stress > 150MPa.

Figure 6 shows film stress stability for both compressive and tensile TEOS SiO films deposited at < 190°C and then left exposed to atmosphere at room temperature of up to 50 hours. Stress is stable for both compressive and tensile films.

The electrical properties of tensile TEOS SiO films are seen to degrade as the tensile stress increases.

Figure 7 shows leakage current vs electric field strength for compressive and tensile TEOS films. High field leakage is increased for films with low tensile stress (+66 MPa) and leakage at 2MV.cm⁻¹ increases by a decade as the stress is increased from +66 MPa to +200 MPa. The electrical and cracking threshold data suggest that if TEOS SiO is to be used in a passivation stack with net tensile stress, then film thickness should be <1.5µm and stress < 100 MPa.

Tensile silicon nitride films were also investigated as a means of increasing the cracking threshold and providing improved electrical properties compared to TEOS SiO and so thereby offering greater tensile stress compensation capability. A <190°C SiN film was developed with tensile stress of +200 MPa and cracking threshold >7µm. The cracking threshold was demonstrated for films deposited on to bare Si and also on to a compressive SiN barrier film.

Figure 7 shows stress stability of 1.4µm low temperature SiN films with nominal 200 MPa tensile stress. After 100 hours of exposure to atmosphere at room temperature, the stress has shifted by less than 5%.

Figure 8 shows electrical performance of low temperature SiN films with stress ranging from -400 MPa to +200 MPa. Leakage at 2MV.cm⁻¹ is comparable for all films, with high field leakage increasing as tensile stress increases.

The cracking threshold, stress stability and electrical performance suggest that low temperature SiN films are more suitable than TEOS SiO films for via-reveal passivation stacks where a net tensile stress is required.
Figure 10 shows cross-sectional SEM images of a via-reveal passivation stack deposited over a silicon pillar to demonstrate step coverage. The stacks consists of 0.21µm compressive SiN (-100 MPa) with 2.25µm tensile SiN (+200 MPa), these stress values having been measured on full thickness silicon wafers. Adhesion of the compressive SiN film to silicon, and of the tensile SiN film to the compressive SiN film is excellent. Such a stack can provide near-full bow compensation on CMOS wafers with incoming tensile stress.

Conclusions
Low temperature (<190°C) PECVD SiN and SiO films are shown to be well suited for use in via-reveal passivation stacks. Novel processing suppresses moisture re-absorption in low temperature TEOS SiO films, thereby providing stable electrical and mechanical performance, with no drift over time. Low temperature TEOS SiO films are more suitable to applications where a compressive stress is required due to cracking threshold thickness limitations. Stable SiN films can, however, be produced with a tensile stress and cracking threshold of >7µm. These films are useful where incoming tensile stress must be compensated by the back-side via reveal passivation stack.

References