Impact of Backside Processing on C-V Characteristics of TSV Capacitors in 3D Stacked IC Process Flows

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Abstract
In this paper, we describe the importance of carefully selecting the wafer backside processes in 3D stacked IC process flows. In particular, we report on the impact of TSV Via-middle reveal and backside passivation processes on the C-V characteristic of the TSV. The cause of anomalous C-V inversion of the TSV capacitor is explained and a solution is given to avoid this effect.

Introduction
For high-speed data transfer in 3D stacked ICs, the capacitance of the via-middle TSV plays an important role [1]. In this paper, the relation between backside processing steps and the C-V characteristic of a TSV capacitor is described for the first time. It is shown that after backside processing the TSV capacitance rises from the depletion value up to the higher accumulation value, thus going into inversion. This effect potentially increases the RC delay of signal propagation through the TSV and should be prevented.

This paper starts with an overview of imec’s backside process of record in a typical TSV via-middle 3D-IC flow. The C-V behavior of a TSV capacitor structure is then described in details. The backside processing steps are screened and the type of backside passivation deposition is identified as the root cause for TSV C-V inversion: the positive charges trapped in the passivation material during deposition generate an excess of minority carriers (electrons in the p-type silicon), at the substrate backside, which can flow in the positive-biased TSV capacitors and cause inversion in the C-V behavior of the TSV. This hypothesis is confirmed by simulations and experiments. A careful choice of the backside passivation material and of the deposition conditions is therefore essential to mitigate the onset of positive charges and, consequently, the inversion in TSV C-V curves. In this respect, a low-temperature PECVD TEOS layer (deposited at 185°C) in combination with a NH3 free SiN4 layer, is finally proposed as passivation layer preventing the onset of TSV C-V inversion.

Integration scheme

A 5x50μm via-middle TSV is manufactured after contact processing, followed by 2 metal layers in a 65nm BEOL technology and completed with passivation layers and Al metallization. This scheme is the common basis of the further screening of the different steps which may impact the C-V characteristic of the TSV capacitance.

Fig. 1. Backside passivation process flow

CV characteristic of the TSV capacitor

After processing of the wafers, the C-V characteristics of the TSVs are measured. The TSV forms a parasitic MIS (Metal-Insulator-Semiconductor) cylinder capacitor [3], with the TSV plug as metal electrode, the liner oxide as insulator and the Si substrate as semiconductor (Fig. 2). The

capacitance of a MIS capacitor is known as being voltage dependent: the typical capacitance vs. voltage characteristic (also known as the ‘C-V curve’) shows a high capacitance value in the accumulation region and lower capacitance in the depletion region, when measured in the kilo-hertz frequency range. For a p-type substrate, the lower TSV depletion capacitance appears when the TSV is connected to positive voltages, i.e. digital signals set at “1” or power supply of the 3D-IC where the TSV provides electrical connection with other ICs in the stack. The 2 operational modes of the TSV capacitance are depicted in Fig. 2.

![Fig. 2. Parasitic MIS capacitance formed by a TSV and typical CV curve of a TSV formed capacitance.](image)

To characterize the TSV capacitance, the 50µm thick wafer was peel debonded to a dicing tape, this in order to have access to the measurement pads on the front side of the wafer.

**Analysis of C-V characteristic of the TSV capacitor during backside process steps**

In this section we report on the influence of the different backside processing steps on the TSV C-V curve. Before the backside processing, the TSV C-V curve was measured at 10kHz after the front-side integration on a full-thickness wafer. The curve is the expected CV characteristic of the TSV in a p-type substrate (Fig. 3). For negative voltages the TSV is in accumulation and the capacitance value is about 140fF, for a TSV with a 200nm oxide liner. After grinding the substrate, with about 10 µm of silicon left above the TSV, the shape of the C-V curve is preserved, deep depletion is still observed for positive voltages and no inversion appears.

![Fig. 3. TSV C-V curve - TSV fully embedded in Si](image)

After revealing the TSVs by a HF/HNO₃ and TMAH wet etch, the deep depletion disappears, as depicted in Fig. 4. This indicates that the wet TSV reveal process introduces traps in the depletion region, leading towards a reduction of the minority carrier lifetime. The TSV capacitance slightly increases as compared to deep depletion, but it is still much lower than the accumulation value.

![Fig. 4. TSV C-V curve after TSV wet reveal, deep depletion disappears.](image)

Fig. 5 shows the measured C-V characteristics of a TSV after deposition of the 500nm low temperature PECVD Si₃N₄ passivation layer. For negative voltages, the TSV is in accumulation. For positive voltages, the capacitance is at the higher accumulation value. This unexpected inversion increases the capacitive load during data transfer through the TSVs and should therefore be avoided.

![Fig. 5. TSV CV curve after 500nm PECVD Si₃N₄ backside passivation deposition](image)
Avoiding anomalous inversion of C-V characteristic of the TSV capacitor

Although wet TSV reveal process is claimed to be more cost effective [4] the imec current process set-up does not offer end-point detection. This makes the process difficult to control as multiple reworks are very often required to achieve the target TSV nail height and to cope with non-uniformities introduced by variations of TSV trench depth and Si thickness after grinding. The performance of TSV reveal by an SF$_6$-based dry etch process was evaluated on a 300nm SPTS Rapier XE system. The process combines high RF source power (~8kW) with high gas flow to maximize the Si etch rate at about 9.4 µm/min. Uniformity is controlled by a ‘dual source’ design [5], separating the RF powers and gas inlets into primary and secondary locations. The dry etch chamber includes an in-situ end-point detection (ReVia®) system. The Si etch is highly selective to oxide.

A more detailed comparison on the wet and dry soft TSV reveal and their performance is described in [6]. The impact of the TSV reveal by dry etch on the C-V characteristic is presented in Fig. 6. It is clear that besides the process advantages, the dry etch reveal on the SPTS Rapier XE is preserving the deep depletion, thus not introducing any traps in the depletion region of the TSV capacitor.

![Fig. 6. TSV C-V curve after TSV reveal by SF$_6$ based dry etch, normal C-V curve](image)

Imec’s process of record for backside passivation is a low temperature (180°C), 500nm thick PECVD nitride layer. This layer is causes anomalous inversion of TSV capacitor, as shown in Fig. 5. This deposition uses silane SiH$_4$ and ammonia NH$_3$, thus introducing many positive charges in the film due to the high hydrogen content. The positive charges in the nitride layer on the backside of the wafer cause inversion of the backside silicon surface and forms an unlimited source of negative minority carriers. These charges flow into the Si-liner interface and cause the inversion of the C-V curve of the TSVs (Fig. 7).

The hypothesis of positive charges in the nitride layer on the backside causing inversion was validated by simulating the TSV capacitor with Sentaurus (Synopsys). To reduce the simulation time, the diameter of the TSV was reduced, resulting in a lower capacitance value. It is clear from Fig. 8 that by increasing the positive charge $Q$ of the backside passivation layer, the capacitance value for positive voltages tends towards inversion.

![Fig. 7. TSV capacitor inversion caused by poor quality BS passivation](image)

![Fig. 8. Simulated TSV C-V curve with increasing number of fixed positive charges in the backside passivation layer](image)

More detailed simulations with a different software package confirm this result [7]. To verify experimentally the hypothesis of positive charges causing anomalous inversion in p-type Si, we also processed via-middle TSVs in n-type Si. In Fig. 9, the C-V curve is shown for a TSV in an n-type substrate, foreseen with a low temperature (180°C), 500nm thick PECVD nitride layer. For positive voltages the TSV capacitor is in the accumulation region. When sweeping to negative voltages, the capacitor goes into depletion mode. No inversion is observed, since positive charges in the backside
passivation can attract only negative charges in a n-type substrate; no source of minority carriers (holes) is present.

To limit the amount of positive charges in the passivation layer, the hydrogen content of the passivation film needs to be reduced. Both NH$_3$ as SiH$_4$ can contribute to this. First, a SiH$_4$ based low temperature PECVD SiO$_2$ is deposited on the backside. Although no NH$_3$ is used in this process, we still observe TSV C-V inversion (not shown but similar to Fig. 5).

A solution is provided by dielectric films deposited on to 300mm Si wafers using an SPTS Delta xp, single-wafer cluster system, configured with degas and PECVD chambers. Degas is required for temporary bonded wafers to ensure a sufficient outgassing of the bonding adhesive prior to dielectric stack deposition, to prevent consequent disruption of plasma stability and degradation of film properties.

Si$_3$N$_4$ and SiO$_2$ films were deposited in a capacitive-coupled, parallel plate PECVD reactor. The wafers sit on a resistively-heated platen during deposition with temperature adjusted to maintain a maximum wafer temperature of <185°C, as required to prevent premature debonding of the silicon wafer from its temporary carrier.

Silicon oxide films are deposited using a TEOS-based chemistry with dual frequency excitation (13.56 MHz and 375 kHz applied simultaneously with the showerhead). TEOS is preferred to silane as primary precursor, because of its superior step coverage and lower hydrogen content in the deposited film. SiO$_2$ stress is tuneable from -200 MPa to +200 MPa. For this work, the SiO$_2$ deposition process is optimized to prevent absorption of moisture from atmospheric exposure. In fact, SiO$_2$ films deposited using TEOS at low temperature can be hygroscopic and the water absorption causes instability with leakage current and stress drifting upwards over time.

Silicon nitride films are deposited using a silane-based, ammonia-free process chemistry and 13.56 MHz excitation frequency. Film stress is tuneable from -400 MPa to +200 MPa where a negative stress denotes a compressively stressed film. The use of 13.56 MHz (compared to low or mixed frequency processes using 375-380 kHz excitation) avoids excessive ion bombardment of the film and enables high deposition rates without causing overheating of the substrate. This is especially important for bonded substrates, where thermal conduction to the wafer platen is significantly reduced compared to a non-bonded silicon wafer.

SiO$_2$-Si$_3$N$_4$ stacks are deposited sequentially in the same PECVD chamber. Such an approach is preferred for best system productivity. A more detailed description of the deposition system properties of the dielectric layers can be found in [8].

By using a 150nm TEOS-based SiO$_2$ and a 250nm Si$_3$N$_4$ as passivation for Cu diffusion, the C-V curve of the TSV capacitor does not move into inversion for positive voltages (Fig. 10).

**Conclusions**

In this paper, a solution to prevent anomalous C-V inversion effect in TSV MIS capacitors is reported for the first time. This effect increases the RC delay of signal propagation through the TSV and should be prevented. For a typical 3D integration scheme with via-middle TSVs, the backside processing steps are analyzed step by step. The amount of positive charges in the backside passivation layer experimentally verified as being the cause of the anomalous C-V inversion; the proposed solution consisting of depositing a TEOS based SiO$_2$ covered by an NH$_3$ free Si$_3$N$_4$ layer results effective.

**References**

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