High Density Packaging on Wafer Level Fan-out: Deposition and Via Drilling Solutions Tailored for Non-Silicon Substrates

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Contents

■ FOWLP in advanced packaging
  ■ Position in the market
  ■ How it’s made
  ■ How it’s used

■ Processing FOWLP wafers
  ■ Contamination
  ■ Warpage

■ High density FOWLP
  ■ Through mold vias by laser drill
  ■ Metallizing TMV
The Rise of FOWLP

- 3D production starts in 2015
  - 4 die stacked memory
  - SKHynix, Samsung & Micron all announced readiness
- 2.5D ramping for high BW: CPU with stacked memory
  - AMD graphic with SKHynix HBM
  - Intel “Knight Landing” MPU with Micron HMC

- High bandwidth packages with 2.5/3D is now
- When will it move into broader markets?
  - It’s all about cost…

- Could FOWLP fill the gap?
The Interposer Gap: Line & Space

PCB Substrate Manufacturers

OSAT / Wafer foundries

Silicon

Opportunity

FanOut

STATS eWLB: 10µm L/S
TSMC INFO: 5µm L/S
RDL first FO: <2µm L/S

100µm -> 25µm -> 10µm -> ~8-5µm -> 1µm

100nm -> 10nm

Lower cost than Si/Glass Interposer?

Glass
Who manuf interposers?
Ground rules?

Organic Substrate

GAP!

High Cost

Who manufactures interposers?

Ground rules?

Who manufactures interposers?

GAP!

Wafer Design Rule

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Courtesy Phil Garrou, Yole
Mobile is the main driver

Auto, medical, industrial all active

20% CAGR through 2020
Simple FOWLP

- Laminate foil on carrier (Si, glass)
- Pick & place KGD on carrier
- Wafer level compression molding
- Remove carrier, invert mold substrate
- RDL by thin film tech
- Solder ball attach
- Singulate
FOWLP Uses

Partitioning needs to be designed for
- Big die into smaller die means higher yield
- Separating functions means fewer interconnect layers
- Use appropriate nodes for some operations saves $$

RF with small spaced passives
- Better performance in a smaller package
Performance Benefits of FOWLP

- Form factor - <0.3mm height, <0.8mm stacked
- Short die-to-die, die-to-passive spacing, <100um
  - Smaller footprint than pcb mount
  - Speed, heat dissipation
- Low loss substrate, high Q factor inductance
- >60 GHz capable
  - HD video streaming, fast file transfer
RDL Processing on FOWLP

- FOWLP mold RDL processing has two main challenges:
  - Contamination
    - Mold contains moisture, solvents
    - Must be removed before metal dep otherwise high Rc
    - Problem: mold wafer max temperature is <150°C
    - How drive out contaminants at low temperature?
  - Warpage
    - Mold wafer is not flat
    - Mold getting thinner to save costs, reduce height
    - Different die placement patterns change stress
    - Problem: how cope with up to 6mm warpage?
Sigma fXP PVD System

- 200/300/HD Wafers
- Industry Standard EFEM
  - Up to 3 Load Ports
- Vacuum Transport Module
  - Cryopump vacuum
- Up to 6 Process Modules
Mold Contains Contaminants

- Water and CO dominate
- At 120°C, takes @30mins for gases to approach pre-load values
- How manage and still be productive?
Multi-Wafer Degas (MWD)

- Vertical batch degas module
  - Integrated to cluster tool
  - No vacuum break; degas to dep
- 200/300/HD wafer sizes
- Tmax 150C
- Cryopumped for water efficiency
- Complex scheduling software
  - Manages batch/single wafer interaction

Up to one hour degas time for each wafer
BUT with batch, a degassed wafer is available every 90secs
Continuous processing of 25x300mm wafers

<<10secs to achieve E-08T. No upward trend

Contamination free background
Rc Sensitivity to Degas Time

Tests performed on FO-WLP Epoxy Mold Compound Test Vehicle
TMAX = 120C

Benefit of batch degas:
Longer degas, no loss in t’put

Rvia drops as increase degas time

35 mins
Handling Warped Wafers

- Building on experience with Power BSM…
- Modifications for thin wafers:
  - Chamber furniture clearances
  - Robot acceleration/deceleration profiles
  - Wafer lift acceleration/deceleration profiles
  - Slot pitches
  - Temperature rise & fall rates
- Ability to cope with…
  - Mold thickness 800 um, trending to <400um
  - Warpage 3mm, trending to >6mm
Increased Density: FOWLP with TMV

- High density POP, or use both sides of substrate
- Laser drill through 200 to 400um EMC
- 80° taper to near vertical vias
- Highly accurate registration
- High speed for dense drilling patterns
Emerald Laser Via Formation

- 8 steering mirrors = 8 drilling channels
- Continuous drilling
  - No waiting time for mirror reposition
  - 100% utilization of laser
  - Drill speed increases with via density
- UV laser source
  - Smaller wavelength, better resolution

Drilling Speed vs Via Count

Multi Path Technology - parallel

Conventional laser drilling - serial
Multi Path: Cooler Technology

Volcano and mushrooming due to overheating

One laser per substrate risks overheating via

8 beams – parallel drilling. No overheating

Smooth walls
Local and Global Accuracy

- Connect system to fab CAM
  - New layouts available in <5 mins
- <5um drill accuracy wafer to wafer
  - 2 to 3x tighter than competition

4000 measurements over 1 week, multiple substrates
Laser Drilled Vias

- Down to 50 um diameter with UV wavelength
- Vertical and tapered
- Reduce beam energy as approach base
  - No damage to Cu pad
Metallizing Laser Drilled TMV

- Epoxy Mold Compound
- 250 µm x 560 µm Via, AR2.2
- Deposited Film Stack:
  - Ionized PVD barrier/seed
Summary

- 2.5/3D production starting now
  - High bandwidth applications

- When will technology be applied to broader end markets?
  - COST…
  - FOWLP a promising alternative

- FOWLP presents new challenges to equipment vendors
  - Contamination must be removed at <150C
  - Warpage up to 6mm

- New technology developed for RDL PVD
  - Batch style degas and large bow handling

- UV, multi beam laser for high density TMV
  - Small diameter vias, smoother sidewalls
  - High rate drilling without exceeding temperature budget

- Ionized PVD into laser drilled TMV verified