ABSTRACT
Plasma dicing is attracting significant interest within the semiconductor industry as a viable alternative to conventional singulation methods using saw blades or LASERs. Using Deep Reactive Ion Etch (DRIE), also known as the “Bosch Process”, trenches are etched through the silicon wafer between each die.

This paper describes the current state of the art for DRIE plasma dicing techniques and highlights the advantages of employing an endpoint solution to protect die integrity and the exposed tape at the end of the etch.

Pre-definition of the dicing lanes is the key challenge in full integration of plasma techniques. Means by which the dicing lanes can be prepared for the plasma process will be discussed. The impact and management of exposed metals on the device surface, such as solder bumps and bondpads will also be presented. Approaches that combine conventional and plasma dicing methods will be reviewed.

Key words: plasma dicing, silicon DRIE, dice after grind

INTRODUCTION
Plasma dicing promises significant benefits in increasing wafer throughput, die per wafer and die yields (due to low damage processing). For small die, in particular, where the time required for a high number of mechanical slices in “series” can be substantial, a “parallel” process such as plasma dicing which etches all dicing lanes simultaneously, can significantly increase wafer throughput.

Maximum benefits can be gained for brand new production schemes where plasma dicing is “designed in” from the beginning. This allows the device designers to layout the devices and test structures on the wafer in the most efficient way, with the added flexibility that die shapes need not be constrained by the straight cutting paths of a mechanical saw. With dicing lanes defined by photolithography, these lanes can be narrower than the width of a dicing blade, saving valuable silicon real-estate which can be used to increase the number of die per wafer. Also, when designing a new device/wafer layout, a designer can make sure that dicing lanes can be free from metals and other layers which can hinder plasma etching. This is often quoted as the prime challenge which prevents implementing plasma dicing in an existing production scheme.

However, even with existing processing routes, certain benefits can make plasma dicing an attractive alternative to mechanical saw or LASER solutions. Plasma dicing is non-damaging and can produce die with improved strength compared to a traditional saw. Plasma dicing is also attractive for fragile devices such as MEMS, since there is no physical force to vibrate the wafer, in contrast to forces applied in a saw process.

This etch process can either be carried out before grinding, where the wafer is only partially etched and singulation occurs when the remaining silicon is mechanically ground away, or after grinding in the more traditional scheme where singulation takes place during the dicing step.

DEEP REACTIVE ION ETCH PROCESSING
Deep Reactive Ion Etch (DRIE), also known as the “Bosch Process” is an dry etch technology which uses alternating cycles of surface passivation using a C4F8 plasma, followed by an SF6 plasma with directional ion bombardment to expose silicon at the base of the feature and a short (isotropic) etch which deepens the features, without etching the sidewalls of the hole, which are still protected by a passivation layer. These 3 steps (shown in Fig 1 above) are repeated many times to produce vertical high aspect ratio via holes.

The isotropic nature of the SF6 etch of the exposed silicon at the bottom of the feature, in each step, can lead to characteristic “scallops” on the sidewall as the etch progresses deeper into the silicon. To minimize this effect, it is necessary to use very short etch cycles so that the size of a single scallop associated with each etch cycle is reduced to a minimum to create an essentially smooth surface. Shorter etch cycles reduce the overall etch rate which has a detrimental effect on the throughput for MEMS manufacturers, so a balance between the need for high etch rates (for higher throughput) and the appearance of the scallops on the sidewalls.
CHALLENGES OF PROCESS INTEGRATION
Compatibility with commonly-used tapes/frames
When introducing a new process technique, it can be more difficult if it requires changes to established protocols or uses new or novel materials. A DRIE solution for dicing would not be totally unfamiliar to frontend fabs and users. However, it presents a new set of criteria to backend fab users, and the frontend vendor also needs to take account of the substrates and protocols used in this area including; materials of substrates, treatment of material and the potential recovery of broken wafers.

The most significant aspect of the framed substrate is the tape as it serves as the sole preserver of mechanical integrity for the wafer before and after singulation. In order to ease the introduction of plasma based dicing, accommodation of existing tapes, and frames, was the primary aspect included in the SPTS design brief. No element of bespoke material was considered due to the breadth of the existing infrastructure and the likely resistance to significant change. So an understanding of the materials is paramount to ensure the DRIE system can manage them successfully. When considering the conditions the backend substrate, and therefore the tape, has to endure it is wise to understand how the tape would behave. For such an established process step as singulation, it can be surprising how many variables there still are when considering the tapes available. This is a reflection of the breadth of device types now being fabricated across the industry.

Within this range of tapes the decision matrix requires consideration of the flexibility of the tape for the separation of die after singulation and the temperature resistance of the tape for the etching step.

The tape producers have many off-the-shelf options that meet the demands of both of these aspects, meaning that there are several existing materials that have distinct advantages for plasma dicing.

<table>
<thead>
<tr>
<th>Tape Product</th>
<th>Melt</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>PET = Polyethylene terephthalate</td>
<td>250°C</td>
<td>Resin-based 70°C glass temperature</td>
</tr>
<tr>
<td>PVC = Polyvinylchloride</td>
<td>~160°C</td>
<td>&gt;Thermoplastic -82°C glass temperature. Decomposes at ~140°C</td>
</tr>
<tr>
<td>PO = Polyolefin</td>
<td>~55-110°C</td>
<td>Thermoplastic – softens 20°C below melt</td>
</tr>
<tr>
<td>PI = Polyimide (Kapton)</td>
<td>-</td>
<td>Ok to ~450°C. Shrinks 1% @400°C</td>
</tr>
<tr>
<td>PA = Polyamide (Nylon)</td>
<td>190-3501°C</td>
<td>Thermoplastic – 190°C glass temperature</td>
</tr>
</tbody>
</table>

Table 1. Variety of the tape materials used and some of their properties.

Notch Elimination
When etching down to a tape, in the case of “Dice After Grind”, the conditions are very similar to etching an underlying oxide layer in a “silicon-on-insulator” (SOI) wafer, commonly used in MEMS manufacturing. Generally the non-uniformity of the plasma process and/or wafer itself will result in some areas of the underlying oxide or tape being exposed before other areas. This means a short “over-etch” period may be required to ensure the process is complete across the whole wafer. During this over-etch period a build-up of charge can occur on the exposed non-
Conductive layer, which will deflect ions laterally into the sidewall of the feature causing a notch at the bottom of the etched trench (See Figure 2, below).

**Figure 2.** Notching at interface of silicon & buried layer

Normally, when considering the interdigitated fingers of an inertial MEMS device, some notching can be accommodated. However, when the phenomena is transferred to the underside of an active device which is being picked and placed onto a tape reel or other such receptacle, then the risk of damage or compromise is much higher. Furthermore, there is evidence to suggest the lack of process control leading to notching under the die can adversely affect die strength.

To prevent notching (and at the same time, protect the tape & die) it is imperative to carefully control the etch conditions at the base of the dicing lane, as the tape is exposed. Generally, the process can change to a discrete set of overetch conditions once the endpoint has detected the tape has been reached. Normally, this will be a slower, less aggressive step.

To avoid slowing the etch rate too soon, which would reduce throughput unnecessarily, in-situ endpoint detection is required. Narrow dicing lanes mean there is a low exposed silicon area, which can pose a challenge to most endpoint techniques. SPTS developed Claritas (6) to provide clear endpoint capability even when the open area of a wafer was <1%. In the case of plasma dicing, the open area has been observed down to <0.001%. Claritas is able to detect a sufficiently strong signal change, at this level.

One of the techniques developed when the Bosch process was first introduced for SOI wafers was a management of the standing charge by pulsing the bias RF during the etch. By having the RF off for a period of time during each of the Bosch steps, there would be time for the charge to dissipate. This would prevent deflection of incoming ions and reduce the lateral erosion and hence the notching.

In combination with the pulsed bias RF, use of endpoint is critical in avoiding the creation of notching. By detecting that the etch front has reached the tape as early as possible gives the maximum possible headroom to apply the most appropriate overetch. The ability to apply endpoint detection to the overetch step itself could also further protect the device and tape.

More importantly, the tight process control gained from this will improve throughput, eliminating costly extended timed etches. The images (Figure 5) below compares examples where endpoint is used to control the last stage of the dicing etch and the damage that can occur of the etch is not endpointed/controlled.
Requirements for Dicing Lanes

Pre-definition of the dicing lanes is the key challenge in full integration of plasma techniques. The impact and management of exposed metals on the device surface, such as solder bumps and bondpads has been investigated, in addition to new approaches that combine conventional and plasma dicing methods.

A substrate to be patterned for dicing may include a number of characteristics which can cause issues for a conventional lithography step, i.e. existing patterning, thinned wafers (<200μm), surface topography, and potentially mounted on to tape frame. Photolithography can still be included as an option. However, some users may not want the additional steps and associated costs to be added at this stage of the process flow. As per any “normal” silicon etch, use of photolithography with a PR or oxide mask would provide sound patterning for the etch process. Clearly, sufficient material would be required in order to cope with the selectivity of the etch process and any surface, including solder bumps.

For certain categories of device; e.g. silicon submounts, chipcard and PV, the photolithography approach should be the default choice. However, for memory, logic and some MEMS, these require some tangential thinking to provide a defined lane ready for the plasma etch to take place. None of this would affect material within the lanes that could have an impact on the integration of plasma dicing. Current plasma dicing technology is based on silicon DRIE etch and whilst the process modules, such as SPTS’ Rapier-S, can also do a reasonable job of etching dielectric layers they cannot etch metals. In fact, the chemistries and conditions required for etching metals are not typically compatible with the tapes and frames utilized in the singulation process. Without any additional steps, it is possible to produce defined lanes simply by modifying steps earlier in the process flow, potentially also dealing with the metals issue at the same time. It is suggested that with minor modifications to the mask layouts, removal of the metal and dielectric materials from the lanes can be undertaken at the patterning steps, as they occur throughout the process flow.

By considering that to adopt this would require designer time and mask sets, it would be a one-off cost. However, this would have the secondary effect of eliminating the test structures that normally occupy the dicing lane rather than taking up die footprint. This would be a problem and could prevent this scheme from being used. There are two ways of counting this aspect. Benefits of moving to DRIE for dicing have been reported elsewhere (4, 5, 7) and several of these pertain to the ability of designers to free up real estate by narrowing lanes and changing die shape and arrangement. With this in mind, it would be possible to move the test structures into a region previously used for devices. E.g. For 1mm² die, a reduction in lane width could see approximately 20% increase in die per wafer. It is easily conceivable that it would be possible to convert some of those additional die locations into test structures and still retain almost all of the gain from the design change. This would allow use of the option to retain the existing “upper” materials as mask and definition for the dicing lane etch.

The alternative approach is to use a combination of the existing blade and/or laser dicing and plasma to effect the singulation. Irrespective of the material in the lanes, there have always been blade and laser solutions for singulation. This can be advantageous when considering definition of lanes for DRIE. It is the impact on die integrity that is the major detractor for the conventional methods. But, when considering them as a “direct write” for defining the lane for subsequent plasma etch these issues should not come into play. The chipping related to blade dicing would only occur when considering the cut through the whole wafer thickness, this need not be the case when only a cut through the upper layers, stopping at the silicon, is completed. Using laser to ablate the upper layers followed by a “clean-up” of the debris using a blade can also be an option. Neither technique requires an additional masking step with the normal co-
ordinate control and alignment of conventional dicing systems applied. Of course, throughput and cost should be considered for the adoption of this approach. Nonetheless, this technique has been demonstrated successfully provided another option for adopting plasma dicing.

EFFECT OF METHOD OF DICING LANE PRE-DEFINITION ON DIE STRENGTH

Previous work has theorized that a low damage plasma etch process would result in stronger die and improved die yield. In this work SPTS & DISCO have investigated the hypothesis in greater detail to quantify the difference in die strength a range of plasma dicing processes to compare the effects of notch size and sidewall roughness.

Also, many users will wish to avoid an additional and relatively costly photolithography step, or have non-silicon layers in the dicing lanes which need to be removed before plasma dicing. Therefore we investigated using both mechanical saw and laser etching to pre-define the dicing lane prior to plasma etching. Neither technique requires an additional masking step, but the user would compromise some of the benefits, e.g. limiting ultimate minimum dicing lane width, restricting use of the more flexible die shapes and some of the potential for increased throughput.

Figure 9 Chart showing die strength comparison between singulation techniques with varying patterning methods

It is clear from Figure 9, above, that there is an improvement in die strength from plasma dicing techniques approximately twice that from the conventional blade or LASER methods. There is some variation due to the patterning method adopted, but not overly significant.

A key result is that of the plasma diced structures where a notch under the die has been generated. This is to replicate a scenario where endpoint detection and process control during the over etch is lacking (As see in Figure 5). Here, the die strength is lower than that from the conventional singulation techniques.

It highlights that the advantages of plasma dicing can be heavily compromised if the actual execution does not include such capability as that derived from endpoint control (i.e. SPTS’ Claritas) or management of the overetch with pulsed bias and other process considerations.

CONCLUSION

Although integration of plasma dicing into current process flows is in its infancy, there is no doubt that plasma dicing will become widely adopted as it continues to mature and more users take their first steps in trialling this technique. What is clear is that designing in plasma dicing from the outset of a device life cycle is perhaps the only way to benefit from all of the benefits that plasma dicing can provide.

However, it has been proven that considering novel approaches within current device process flows, plasma dicing can be immediately adopted and there are significant advantages from doing so, namely in device quality.

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REFERENCES