EXTENDING CAPABILITIES OF ETCH AND DEPOSITION TECHNOLOGIES FOR 3D PACKAGING OF MEMS IN VOLUME PRODUCTION

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ABSTRACT
This paper highlights a number of challenges and solutions developed to meet the needs of MEMS manufacturers using 3D packaging for low I/O count devices.

Various process steps, such as, TSV etch, dielectric liner deposition, barrier/seed PVD have been developed and optimized to increase electrical performance, increase throughput and reduce costs for volume production.

In particular, various silicon etch processes have been developed to create a wide range of TSV profiles, both tapered (allowing relatively simple deposition processes) and vertical (reducing real estate). Unique endpointing techniques have also been proven in production for both tapered and vertical vias.

Low temperature PECVD is also a key process, for depositing via dielectrics onto bonded wafers with a low temperature (<200°C) threshold.

Finally, this paper illustrates some of the challenges regarding barrier/seed deposition using conventional PVD, and ionized PVD and how technologies such as MOCVD may be useful.

Key words: MEMS Packaging, TSV etch, silicon DRIE, low temperature PECVD, high aspect ratio PVD.

INTRODUCTION
Low I/O devices used in modern smartphones, such as MEMS and CMOS image sensors are increasingly packaged by WLCSP methods to minimise package size. With Through Silicon Via (TSV) schemes, vias are etched from the back of the wafer to contact the sensor on the frontside. This is referred to as “via-last” integration, because the TSVs are formed after device fabrication. Tapered vias are often used to simplify integration with subsequent dielectric and metal lining steps, however, the constant pressure to reduce package size means that via sidewalls are trending towards the vertical. This paper identifies and discusses some of the issues facing manufacturers using ‘via-last’ processing in volume production, and the latest capabilities of etch and deposition technologies to address the requirements of this application.

PROCESS CHALLENGES FOR VIA-LAST
Controlling TSV etch profile
Previous work[1] has shown how plasma etching can be used to create a variety of via profiles.

The Bosch or Deep Reactive Ion Etch (DRIE) process[2] has been used for many years within the MEMS industry. The approach was readily adopted as the accepted means of achieving deep, vertical etched features in silicon. The DRIE process is also becoming the prevailing technology for 3D via production where the extensive experience gained from etching deep MEMS structures is being successfully applied to the etching of TSV structures.

The “switched” Bosch process is a plasma technology which uses alternating cycles of surface passivation using a C₄F₈ plasma, followed by an SF₆ plasma with directional ion bombardment to expose silicon at the base of the feature and a short (isotropic) etch which deepens the features, without etching the sidewalls of the hole, which are still protected by a passivation layer. This process can produce vertical high aspect ratio via holes. The isotropic nature of the SF₆ etch can lead to characteristic “scallops” and mask-undercutting which can make subsequent deposition steps extremely difficult or impossible. To minimize this effect, it is necessary to use very short etch cycles so that the size of a single scallop associated with each etch cycle is reduced to a minimum to create an essentially smooth surface. Shorter etch cycles reduce the overall etch rate which has a detrimental effect on the throughput for MEMS manufacturers, so a balance between the need for high etch rates and a sidewall which will not cause issues with subsequent deposition steps, must be reached by careful process control.
Although vertical vias take up less “real-estate” on the wafer, they are more challenging for subsequent dielectric deposition and metal barrier/seed layers and ultimate copper filling. Therefore, in some cases, tapered vias may be preferred to reduce costs of these subsequent steps.

To create a tapered via the plasma is not switched between separate etch and passivation cycles, but the plasma contains a mixture of etchant (SF₆) and passivating/oxidising (C₄F₈ and/or O₂) gases. A pure SF₆ plasma would isotropically etch the silicon creating an undesirable over-hang underneath the mask and bowed feature shape which would be impossible to deposit onto afterwards. The addition of the C₄F₈ and O₂ is used to control the via profile preventing excessive etching of the sidewalls.

SPTS offers two unique methods for endpointing tapered and vertical vias.

For tapered vias, we have demonstrated that reflectometry[3], using collimated light shone through the plasma and reflected back to an OES can be used effectively in production environments to produce consistent and repeatable results. This method is effective to via densities<1%.

Accurate endpointing of a tapered etch can also enable a controlled amount of over-etch to occur. This is important as the over-etch time defines the top and base dimensions of the final via.

Endpointing tapered and vertical via processes

Endpoint detection (EPD) is important to manufacturers to provide consistent process control for better reproducibility and high yields. In via-last applications, the via etch typically ends at one of the front-side circuit layers (such as oxide or a metal pad). The challenges for endpointing the via etch however, are due to the extremely low exposed area, and in some cases the high aspect ratio features limiting the use of conventional OES (optical endpoint spectroscopy) and interferometry.

Endpointing using reflectance as intensity of reflected light changes as the etch reaches the stop layer

(a)
For vertical vias, we have developed an endpointing system called Claritas™ which is capable of endpointing high aspect ratio features, during DRIE processing, down to a low via density of <0.05%.

As explained above, the DRIE process, continuously alternates between silicon etching and polymer deposition cycles. The end-point detection therefore needs to be ‘gated’ so as to only take an appropriate section of each etch step. Secondly, if the open area is low (<5%) the signal change at end-point is naturally reduced. Thirdly the relatively high pressures used, in order to drive up the etching rate, tend to force the etch by-products into inaccessible regions of the process chamber and/or remove the excited electronic states that cause those species to emit. This latter effect occurs irrespective of open area. For these reasons standard OES set-ups cannot easily detect endpoints across a broad range of practical deep silicon etches required for MEMS devices or 3D-IC stacks requiring through silicon vias (TSVs).

Claritas™ is based around a conventional CCD array OES spectrometer but also uses a proprietary combination of (commonly available) hardware and software algorithms. The result is a gross magnification of signal intensity drop beyond that available from any competing technique[4].

Claritas™ improves wafer yields through the provision of repeatable end-pointed processes wafer to wafer and batch to batch, and eliminates or reduces the need for costly and destructive cross-sectional wafer analyses to check on etch rates.

**Buried Oxide (BOX) Etching**
If required, a limited amount (<2µm) of buried oxide at the bottom of the via can be etched using the same hardware as the silicon TSV etch, saving capital costs for device manufacturers. Claritas™ can also be used to endpoint this process. Thicker bare oxides are normally etched using a dedicated oxide etch module, such as SPTS’ APS.

**Stress control of PECVD dielectrics**
Following TSV etching, a dielectric liner is deposited to provide electrical isolation between the via metallization and silicon. Spin-on polymers were widely used in the earliest implementations of tapered, via-last TSV but PECVD silicon oxides and nitride layers are being increasingly used because of superior stress tuning capability and suitability for vertical TSV. With the trend towards thinner die, the ability to modify the stress of PECVD dielectrics is valuable; particularly for stress sensitive devices such as MEMS.

**Low Temperature PECVD for via dielectrics**
In via-last applications, the thinned wafer is usually temporarily bonded to a glass or silicon carrier and all processes must work below the debond temperature; typically 190°C. In the case of certain sensors, such as magnetometers which contain oxidation-sensitive NiFe components, the MEMS device itself can be detrimentally affected by high temperatures.

Low temperature (<250°C) PECVD films are typically of low density and contain precursor remnants of carbon and hydrogen. This typically results in high wet etch rates, low density and consequently, poor passivation performance. Such films also usually have excessively high leakage currents and this makes them unusable in TSV applications where electrical isolation between via metallization and the silicon substrate is required.

Recent work[5] has described a unique low temperature (<200°C) TEOS-based PECVD process that can deposit SiO into vias with 4-5x better step coverage than silane-based SiO films deposited at the same temperature. Step coverage is important when isolation liners are deposited over the scalloped sidewalls produced by DRIE processes. These films exhibit excellent electrical properties and stability over time (see Fig 6).

**Figure 5.** Reflectance graphs from (a) 200mm and (b) 300mm wafers, illustrating clear endpoints in 1st derivative intensity change

**Figure 6.** Stable leakage current measurements from a wafer coated with low temperature TEOS SiO measured over 9 days.
Metal Barrier/Seed Deposition into via
In applications with heavily tapered vias, standard aluminum alloys are used as the principal conductor. Conventional sputtering is used, a “line of sight” process perfectly suited for depositing into tapered structures. Vertical vias often switch to a Cu-based metal scheme, where PVD is used to deposit seed metal only. Partial or complete fill with metal being achieved using Cu ECD.

For vertical vias with higher aspect ratio, conventional PVD is replaced with ionized PVD to meet the step coverage requirements in deeper, more vertical vias.

I-PVD becomes more expensive for deeper vias. Material costs increase as step coverage reduces, since barrier/seed minimum thicknesses need to be maintained. Throughputs deteriorate and CMP removal costs increase because of the increase in field thickness. As aspect ratios increase and CDs reduce, ionized PVD runs out of steam. MOCVD or ALD techniques delivering conformal metal coverage are the obvious industry-standard alternatives.

However, the majority of processes using these techniques run at high temperatures (> 400°C), incompatible with ‘via last’ TSV schemes that are based on thinned, bonded wafer processing. This has driven the need to develop a ’universal’ deposition technology, compatible with all TSV process schemes, including running at temperatures compatible with via last bonding adhesives (~200°C).

An MOCVD TiN Barrier scheme has been developed that gives >50% step coverage into 8:1 AR vias, at temperatures less than 200°C. This process offers superior sidewall coverage to I-PVD in general, but also allows for rougher DRIE sidewalls at lower aspect ratios (allowing the use of higher via etch rates for higher production throughput) or laser-etched profiles.

For both etch and PVD steps, reliable clamping of wafers is essential to effectively control wafer temperature and produce consistent process results from one wafer to the next.

In ‘via-last’ schemes the thinned silicon wafer is bonded to a carrier (typically glass) that can present issues with wafer clamping as the thin silicon on a relatively thick, non-conductive bulk carrier is not sufficiently conductive at 13.56 MHz to clamp using conventional ESC designs.

**Figure 8.** Schematic of patented thick dielectric ESC

Much research has been carried out to optimise a thick dielectric ESC, which can successfully clamp (and release) such wafers, which is mechanically robust and allows for wafer-less plasma cleaning to extend MTBC for device manufacturers. This ESC design has been proven for many years in volume production in compound semiconductor applications which often use carriers such as glass or sapphire.

**Solution for out-gassing from bonded wafers in production environments**

The presence of a bond adhesive (or other polymers in the MEMS structure) not only limits the maximum temperature limit, but also introduces issues relating to moisture absorption by the polymer on exposure to atmosphere. This can cause the polymer to out-gas as the wafer is heated during the PECVD or PVD steps. The desorbed gas interferes with the plasma stability and can seriously affect the uniformity and properties of the deposited films.

In particular this can lead to yield losses in die near the wafer edge (see Fig 9), or in extreme cases the wafer will be scrapped.
To overcome this issue it is necessary to degas the wafers prior to the deposition steps. This can be carried out “ex-situ” in a separate vacuum furnace but on exposure to atmosphere the polymers will simply begin to re-absorb moisture again.

Ideally a wafer should be degassed and then transferred to the deposition chamber under vacuum (i.e. “in-situ”), without any exposure to atmosphere. In R&D applications this can be achieved by using a dedicated single wafer degas module, or even degassing in the vacuum loadlock prior to the wafer being transferred to the process chamber.

In volume production however this is impractical and would cause a severe bottle-neck in the process flow. To achieve efficient “in-situ” degassing on a production scale a multi-wafer-degas (MWD) solution has been successfully employed. This allows batch degassing of up to 75 wafers at a low temperature for compatibility with bonded wafers.

In production, throughput advantages of batch degas are greater for longer degas times. Low temperatures tends to extend degas times and as Figure 11 shows, an extended degas time can lead to significant improvements in via performance, in this case, lower via resistance.
This MWD solution uses radiation heat transfer to degas wafer and uses a gentle heating cycle to avoid thermal shock to silicon on glass wafers.

### Integrated process development

When developing a TSV process flow incorporating Etch, PECVD and PVD processes, integration of all chambers types onto one cluster platform is beneficial from an initial equipment cost and footprint perspective. The Versalis™ cluster platform (in either ≤ 200 mm or 200mm/300mm formats) can be used to integrate a mixture of up to 6 process modules, as shown schematically below.

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**Figure 12.** Example footprint of a fully populated Versalis™ cluster system incorporating a multi-wafer degas module, one silicon etch chamber, a PECVD chamber and 3 PVD chambers.

### CONCLUSIONS

This paper gives examples of how etch and deposition process technologies are advancing to meet the current and future needs of MEMS manufacturers, with respect to 3D-TSV packaging schemes.

For TSV etching it is possible the tailor the TSV profile to facilitate subsequent deposition steps and minimise real estate used by the TSV. Tapered and vertical vias can be made in the same silicon etch chamber, and endpointed to provide manufacturers with accurate, automatic process control.

Low temperature PECVD processes have been developed for thinned bonded wafers, which provide stable films with excellent stress control and electrical performance without exceeding the debond temperature limit.

Ionised PVD has successfully extended the capability of conventional PVD for higher aspect ratio vias, but in the future other technologies such as MOCVD may be required.

Multi-wafer degassing has been installed and proven in production. This is an essential capability which significantly increases throughput and film quality when depositing onto bonded wafers.

The Versalis cluster platform enables manufacturers to develop all of these process steps and optimize their own process flow on a single platform, saving capital expenditure at the R&D stage, and reducing time to market.

The drive for better device performance and smaller chips will continue to challenge manufacturers, and the acknowledged benefits of 3D packaging will ensure the use of these technologies will increase within the MEMS and other semiconductor markets.

### REFERENCES


