ADVANCES IN ETCH AND DEPOSITION TECHNOLOGIES FOR 2.5 AND 3D BEOL PROCESSING

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ABSTRACT
This paper discusses the optimisation of plasma etch and deposition processes used in interposer and “via middle” schemes to reveal and passivate through-silicon vias [TSV] on the back sides of 300mm silicon wafers, thereby enabling subsequent contact, bonding and stacking processes. A dual source inductively -coupled etch system with innovative in-situ endpoint control enables highly uniform silicon etch, suitable for high volume production. Following the etch step, low temperature (<180°C) plasma-enhanced chemical vapour deposition (PECVD) is used to deposit a silicon nitride (SiN) / silicon oxide (SiO) stack to provide electrical isolation, bow compensation and mechanical support of the revealed vias.

Key words: 3D Packaging, via reveal, low temperature PECVD, silicon etch, in-situ endpoint

INTRODUCTION
TSVs (through silicon vias) are being widely implemented in place of traditional scaling for increasing device performance and reducing form factor [1,2]. Via reveal occurs after the TSVs are formed, to prepare the vias for redistribution metallization. Recent attention has shifted to such post TSV processing steps.

After completion of the front-side wafer processing, the wafer is temporarily bonded, face down, onto a carrier which can be glass or another silicon wafer. The active silicon is then ground typically to within 5-10 μm of the TSV nodes. TSV wafer thickness, carrier wafer thickness, bond layer uniformity, TSV etch uniformity and back-grinding uniformity all contribute to a significant incoming total thickness variation (TTV), which can cause issues with subsequent process steps.

After grinding, the silicon is dry etched in a process that ‘reveals’ the vias to a step height typically in the range 2-5μm. The silicon etch is required to be selective enough to the oxide liner to prevent exposing the copper metal which fills the via.

After silicon etching the vias are passivated typically with a combination of silicon nitride and oxide before Chemical Mechanical Planarization (CMP) and redistribution metallization.

The deposition processes are optimized to provide excellent electrical isolation with the films having low leakage currents and high breakdown voltages. The deposited stacks are also used to compensate for wafer bow resulting from CMOS front-side wafer processes and so provide a method of preventing excessive bow when the thinned silicon wafer is de-bonded from its carrier.

Figure 1 Schematic diagram showing typical via reveal process flow

ETCH PROCESSING
Silicon etching was carried out using an SPTS Rapier process module as shown in Figure 3 and described elsewhere [3]. The patented dual source design [4] comprises independently controlled primary and secondary decoupled plasma zones and independent dual gas inlets. The reactor delivers high radical concentrations.
with a high degree of uniformity control. The inherent multi-mode operation also allows for uniformity tuning that can compensate for incoming TTV.

**Figure 2** Rapier etch module with dual plasma source

An electro-static chuck (ESC) controls the temperature of the bonded TSV wafers. The combination of the dual source, the temperature uniformity from the ESC and the flow dynamics of the reactor govern the resulting etch uniformity across the 300mm bonded wafer. Via reveal processes are typically operated at 30 mTorr pressure, 5 kW source power and with an ESC set point around 10°C. Bias power is avoided for the selective etch to minimize oxide liner loss.

The process module was fitted with a ReVia™ end-point detection system based on a proprietary technique (patent applied for).

**ETCH REQUIREMENTS FOR VIA REVEAL**

For the silicon plasma etch step, there are a number of challenges which need to be addressed:

1. It is critical to control the etch depth uniformity across 300mm bonded substrates.
2. A high silicon etch rate is required for acceptable cost of ownership in volume production.
3. High etch selectivity between the silicon and the TSV liner dielectric (SiO) is required to prevent exposure of via copper metallization.
4. The surface of the silicon needs to be smooth enough for the subsequent dielectric deposition and be consistent with subsequent inspection metrology or lithography steps.
5. It may also be necessary to tune the Si etch profile to compensate for thickness non-uniformity on incoming wafers, introduced through mechanical grinding.

**Figure 3** SEM image showing tips of vias, etched to a revealed height of ~5μm

Figure 3 is a top-down SEM image showing 10μm diameter vias. In this example, the silicon was etched to a depth of 10μm, giving a reveal height of 4.8μm.

**Silicon Etch Uniformity**

Use of a dual-source ICP design allows some degree of compensation for radial thickness non-uniformity on incoming wafers. By varying the ICP source power ratio, the etch rate profile can be changed from centre-fast to edge-fast. Such compensation can help to minimize overall system TTV, illustrated in Figure 4.

**Figure 4.** Infra-red interferometry measurements showing recipe-controlled tuning using primary/secondary power (a) primary only - centre fast (b) secondary only - edge fast (c) optimised primary/secondary

Figure 5 shows a typical plot of etch depth, measured using infra-red interferometry. Plots are shown for N-S and E-W directions. Average silicon etch rate is >4.7μm.min⁻¹, whilst the etch-rate non-uniformity is ±2.4%, expressed as (half-range/mean) and with 3mm edge exclusion.

**Figure 5** Infra-red interferometry measurements showing non-uniformity of ±2.4% in N-S and E-W directions
**High silicon:oxide selectivity**
The Rapier mode process is highly selective to oxide so that the dielectric liner acts as a mask, keeping the Cu which fills each via, fully protected from the plasma etch. With a typical liner oxide of 200nm, a liner thickness loss of 32nm for a 5µm via reveal equates to selectivity of 150:1 (Si:Oxide). This is achieved since the process does not need to rely on the use of bias power to maintain the Si etch rate. Figure 6 shows a revealed via with intact dielectric coverage.

**Figure 6** SEM image showing; (a) side view image of revealed via and (a) top surface of via tip

**In-situ endpoint capability**
For volume production, it is essential that the point at which the vias are revealed can be detected in-situ. Without endpoint the user has to independently measure the silicon thickness above the TSVs on every wafer and adjust the etch time accordingly; adding cost, complexity and the risk of yield loss in the process flow. After processing, under-etched wafers will need to be re-worked or over-etched wafers scrapped.

The ReVia™ endpoint used in this work has been described in previous work [5]. The capability of this technique continues to be investigated and expanded.

Recent work has successfully monitored very shallow reveal heights (~1µm, see Figure 6)

**Figure 7** SEM showing 10µm wide via tips revealed to a height of 1µm

**DIELECTRIC DEPOSITION**
SiN and SiO films were deposited in a parallel plate PECVD reactor. The wafers sit on a platen configured with resistive heating and air-cooling, the latter to prevent energy from the plasma from overheating the wafer and platen assembly during deposition, and also during plasma cleaning of the PECVD chamber. Peak wafer temperature is verified as being <190°C using thermally sensitive adhesive dots applied to the front sides of the substrates prior to deposition. This approach, unlike thermocouple-based temperature measurement techniques, gives a truer indication of peak wafer temperature as it includes film deposition. The thermally sensitive dots have a sensitivity of ±3°C within the temperature range 180°C to 200°C. SiN and SiO films were deposited sequentially in the same PECVD chamber, this approach being preferred for best system productivity.

SiN was deposited using silane-based, ammonia-free process chemistry with 13.56 MHz RF power applied to the showerhead. Film stress is tunable from ~400 MPa to +200 MPa where a negative stress denotes compression. The ammonia-free chemistry was chosen because it produces SiN films of superior quality at low temperatures. The ammonia-free SiN films have a much reduced wet etch rate, resulting from lower hydrogen content and higher density. This gives the films superior diffusion barrier properties.

SiO films were deposited using a TEOS-based chemistry, this being preferred because of its superior step coverage. SiO stress is tunable from -200 MPa to +200 MPa. For this work, the SiO deposition process is optimized so that deposited films do not absorb water on exposure to atmosphere. SiO films deposited using TEOS at low temperature can be hygroscopic and the water absorption causes instability with leakage current, stress and refractive index changing over time [6,7,8].

Stress was calculated using a laser-based bow measurement system. The electrical leakage current density and breakdown voltage of the dielectric films were measured at room temperature using a metal-insulator-semiconductor (MIS) structure with low resistivity silicon as the lower electrode and evaporated aluminium dots with ~1.5mm diameter as the upper electrodes. Leakage current was measured at 2MV.cm⁻¹ electric field strength and breakdown voltage was measured on 150nm SiO and SiN films with voltage swept from 0V to 200V in 5V increments.

Film thickness cracking threshold was determined by using a diamond tip to score the film at the centre and edge of a 300mm wafer. An optical microscope is then used to check for crack propagation over a period of ~24 hours. Observation of spontaneous crack propagation was seen as confirmation that the cracking threshold had been exceeded.
DEPOSITION REQUIREMENTS FOR VIA REVEAL

Dielectric passivation – typically a SiN/SiO stack – must be deposited at <=175°C to maintain the integrity of the temporary bond. The bonding adhesive will also out-gas inside the PECVD vacuum module, potentially disrupting the plasma and the quality of the growing film.

In addition to the inherent temperature constraints, and other challenges introduced when working with bonded wafers, films must have the following properties:

1) Sufficient thickness to provide mechanical stability to the revealed vias and to give sufficient safety margin for the subsequent CMP process – typically several microns.
2) Must exhibit a low leakage current ensuring good electrical isolation between the silicon and overlying metal conductor.
3) High breakdown voltage for reliability.
4) Highly conformal over the revealed TSV, with no seams in the corner between the horizontal silicon surface and vertical TSV sidewall.
5) High elastic modulus and good adhesion are needed to withstand subsequent CMP processes.
6) The stress of the stack must be tuneable to allow compensation for the incoming wafer bow.

Outgassing bonded wafers

Dielectric films were deposited on to 300mm Si wafers using an SPTS Delta® fxP, single-wafer cluster system designed for high volume manufacturing and configured with multi-wafer degas (MWD) and PECVD chambers as shown in Figure 9.

The MWD chamber uses infra-red lamps to heat batches of 300mm wafers, allowing for degas times of up to 30 minutes with minimal reduction of system throughput. Such an approach is beneficial for bonded substrates, as long degas times ensure that the bonding adhesive is sufficiently outgassed prior to dielectric stack deposition, and can also prevent de-bonding due to thermal shock.

Insufficient degas can lead to out-gassing from the adhesive during PECVD film deposition, with consequent disruption of plasma stability and degradation of film properties.

Figure 10 shows outgassing characteristics of five typical silicon-on-glass substrates. The outgassing rate was measured in a PECVD chamber at base pressure (<20mTorr) and peak wafer temperature was <150°C. The out-gassing rate peaks after ~100 seconds with a further 300 seconds required for the pressure to recover fully. Wafer-to-wafer repeatability is good, compared to the difference in outgassing rate between different adhesive types.

![Figure 10](image)

**Figure 10** Typical bonded wafer out-gassing characteristics

Film stability over time

Figure 11 shows a plot of leakage current density vs electric field for the TEOS-based SiO film. When retested several times over several days, the leakage current vs electric field plot does not change.

![Figure 11](image)

**Figure 11** Leakage current density vs applied electric field for low temperature nitride film, measured over a number of days

Similarly, stress in both tensile and compressive SiO films was found to be stable when remeasured 24 and 48 hours after deposition, illustrated in Figure 12.
Film stress control using SiN-SiO stacks

The PECVD passivation layers also serve to maintain bow of the thinned silicon at manageable levels; ideally less than 10mm to allow the wafers to be handled through subsequent process steps. Full thickness (~770µm) CMOS wafers will typically have wafer bows within the range 100-200µm. When these incoming wafers are thinned to ~50µm to allow for chip stacking, bow will increase to several centimetres, making wafer handling impossible and can also likely causing cracking after debond. The stress of the back side passivation stack can be tailored to compensate for the incoming wafer bow and so produce wafers with manageable flatness after debond. To achieve this, low temperature PECVD films having both compressive and tensile stresses must be available.

For example, CMOS devices with multiple layers of Cu-low k interconnect will typically have a front side tensile stress and so via-reveal passivation stacks with net tensile stress are required to compensate. Compressively stressed silicon nitride films are generally acknowledged to give best diffusion barrier properties, these being widely used in CMOS multi-level metal interconnect schemes [9]. For the via-reveal passivation stack, a PECVD SiN process with peak wafer temperature <190°C and film stress of -100 MPa was used.

For wafers with an incoming front side compressive stress, a SiN barrier with thicker (2-3µm) TEOS over-layer, both compressively stressed, can be used to provide both stress compensation and good sidewall coverage of the revealed TSV.

When the incoming front side stress is tensile, then given the constraint of a compressively stressed SiN barrier layer, it is necessary to deposit thick over-layers with tensile stress to produce a passivation stack with net tensile stress. SiN and SiO films can both be deposited with a tensile stress and the two films have both advantages and disadvantages for via-reveal process integration.

TEOS-based silicon oxide films with tensile stress show excellent sidewall coverage and deposition rate compared to silicon nitride, but maximum thickness is limited by the cracking threshold and leakage current increases as the tensile stress increases [10].

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Tensile silicon nitride films were also investigated as a means of increasing the cracking threshold and providing improved electrical properties compared to TEOS SiO and so thereby offering greater tensile stress compensation capability. A $<190^\circ$C SiN film was developed with tensile stress of $+200$ MPa and cracking threshold $>7\mu$m. The cracking threshold was demonstrated for films deposited on to bare Si and also on to a compressive SiN barrier film.

For a full thickness, 300mm CMOS wafer with 60MPa front side tensile stress, a backside via-reveal passivation stack combining $0.21\mu$m compressive SiN ($-100$ MPa) with $2.25\mu$m tensile SiN ($+200$ MPa) provides an optimal solution of metal diffusion barrier, electrical isolation and bow compensation. Such a stack limits wafer bow to $<5$mm when the 300mm wafer is thinned to 50$\mu$m, so enabling further processing of the thinned substrate.

Conclusions
Etch and CVD technologies for 300mm VR processes have been described. Silicon etch rates $\sim5\mu$m/min, with uniformity $\pm2.5\%$ and selectivity to the liner oxide around $\sim150:1$ have been achieved on bonded TSV wafers. A novel end-point detection method has been introduced which allows control of the reveal height. The dual plasma source design allows uniformity tuning of the process to counteract incoming wafer TTV.

Low temperature ($<190^\circ$C) PECVD SiN and SiO films are shown to be well suited for use in via-reveal passivation stacks. Low temperature TEOS SiO films are more suitable to applications where a compressive stress is required, due to cracking threshold thickness limitations. Stable SiN films can, however, be produced with a tensile stress and cracking threshold of $>7\mu$m. These films, in combination with compressive SiN barrier layers, are effective in reducing net wafer bow to manageable levels on 300mm silicon wafers thinned to 50$\mu$m.

References